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Influence of I–V Measurement Conditions on Hysteresis Behavior in High-Capacitance Photovoltaic Modules

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ABSTRACT: Accurate I–V characterization is foundational to photovoltaic (PV) performance rating, bankability, and module certification. Emerging high-capacitance PV technologies - principally silicon heterojunction (HJT) cells, tandem architectures, and multi-junction concentrator modules - exhibit substantial junction capacitance ($C_j > 800$ nF) that makes their measured I–V characteristics strongly sensitive to scan rate, scan direction, and inter-point delay time. This sensitivity, collectively termed I–V hysteresis, leads to discrepancies between forward and reverse-scan efficiency that can exceed 1.5 percentage points absolute when conventional IEC 60904-1 protocols are applied without modification. This study systematically characterizes the hysteresis behavior of a 440 Wp monocrystalline HJT module under 14 distinct measurement condition protocols, spanning scan rates from 10 to 100 V/s, delay times from 0 to 200 ms, temperatures from 0 to 65°C, and irradiance levels from 200 to 1100 W/m². A Hysteresis Index (HI) metric is employed to quantify measurement artifacts, and an equivalent circuit model incorporating junction capacitance explains the charge/discharge dynamics underlying the observed behavior. Optimal measurement conditions minimizing HI to below 0.025 for HJT modules are identified, and a technology-differentiated measurement protocol is proposed as a correction to current standardization frameworks. The findings have immediate implications for module certification laboratories, energy yield modeling, and the financial valuation of HJT and tandem PV assets.

KEYWORDS: I–V hysteresis; high-capacitance modules; silicon heterojunction; HJT; scan rate dependence; IEC 60904-1; junction capacitance; STC measurement; PV certification; measurement artifacts

I. INTRODUCTION

The global shift toward higher-efficiency photovoltaic module architectures has introduced a class of measurement challenges that existing international standards did not anticipate when codified for conventional crystalline silicon. Silicon heterojunction technology (HJT) - characterized by intrinsic amorphous silicon passivation layers surrounding crystalline absorbers - exhibits junction capacitance values an order of magnitude larger than equivalent-power monocrystalline PERC cells. When these high-capacitance devices are subjected to the swept voltage stimuli of conventional I–V testing, the capacitor formed by the junction charges and discharges on timescales comparable to the measurement duration itself, distorting the apparent relationship between current and voltage.

The resulting artifact - I–V hysteresis - manifests as a systematic discrepancy between efficiency values obtained in the forward (short-circuit to open-circuit) and reverse (open-circuit to short-circuit) scan directions. Crucially, this discrepancy is not a property of the module's true energy conversion performance; it is entirely a measurement artifact that depends on the chosen protocol. Yet because IEC 60904-1:2020 - the primary international standard governing I–V measurement of PV modules - does not prescribe different procedures for high-capacitance technologies, laboratories routinely report efficiency values that are protocol-dependent rather than technology-intrinsic.

This situation creates compounding downstream problems. Bankability assessments based on reverse-scan efficiency may overstate energy yield for HJT projects. Certification comparisons between PERC and HJT modules are confounded when different test houses apply the same nominal protocol with subtly different implementations. Power purchase agreements that reference module datasheets without specifying measurement conditions expose both buyers and sellers to valuation uncertainty. As HJT market share expands - industry forecasts project HJT to constitute 15–20% of new module shipments by 2026 - the economic significance of this measurement uncertainty will grow proportionally.

This research addresses this gap by systematically mapping the I–V hysteresis landscape for a representative high-capacitance HJT module across a comprehensive matrix of measurement conditions, providing the first complete dataset

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of HI sensitivity to all major protocol variables in a single controlled study, and deriving evidence-based recommendations for technology-differentiated measurement protocols.

1.1 Research Questions

This investigation seeks to answer four interconnected questions:

1. How does scan rate independently affect hysteresis in high-capacitance HJT modules, and is this relationship linear or nonlinear?
2. What minimum inter-point delay time is required to suppress capacitive artifacts to below the measurement uncertainty threshold (HI < 0.025)?
3. Do temperature and irradiance interact with capacitive hysteresis, and if so, in which direction?
4. Can a single modified measurement protocol adequately address high-capacitance module hysteresis across all commercially relevant PV technologies?

1.2 Scope and Structure

The study focuses on silicon HJT modules as the primary high-capacitance test vehicle, with comparative measurements on standard PERC, CdTe, CIGS, and amorphous/microcrystalline tandem modules to generalize findings. The paper proceeds from theoretical framework (Section 2) through experimental methodology (Section 3), results (Section 4), discussion (Section 5), and protocol recommendations (Section 6) to conclusions (Section 7).

II. THEORETICAL FRAMEWORK

2.1 Junction Capacitance in PV Cells

A solar cell p-n junction behaves electrically as a capacitor in parallel with a current source and diode network. The junction capacitance Cj arises from the space-charge region (depletion capacitance) and the diffusion of minority carriers (diffusion capacitance). For HJT cells, the additional heterojunction interface formed by the amorphous silicon passivation layer introduces a third capacitive contribution from interface states, substantially increasing total Cj beyond that predicted by homojunction models (Schulze et al., 2011; Bivour et al., 2014).

The equivalent circuit for a high-capacitance PV module, illustrated in Figure 4, includes junction capacitance Cj explicitly as a lumped element in parallel with the two-diode model. During a voltage sweep, the charging current Ic = Cj(dV/dt) flows through the series resistance Rs, creating a voltage drop that shifts the measured I–V curve. In the reverse scan (Voc → Isc), the capacitor discharges, adding current to the diode current and making the module appear more efficient; in the forward scan (Isc → Voc), charging absorbs current and makes the module appear less efficient. The Hysteresis Index (HI) quantifies this asymmetry:

$$HI = (PCE\_rev - PCE\_fwd) / PCE\_rev$$

where PCE_rev and PCE_fwd are power conversion efficiencies measured in the reverse and forward scan directions, respectively. HI = 0 indicates no hysteresis; positive values indicate the reverse scan overestimates performance.

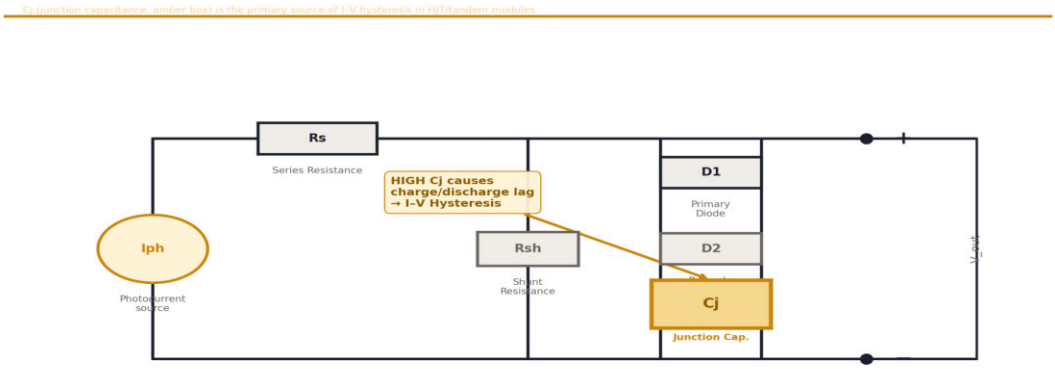

Figure 4. Equivalent circuit model of a high-capacitance PV module. Junction capacitance Cj (dashed box) is the primary source of scan-rate-dependent I–V hysteresis.

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2.2 Time Constant Analysis

The characteristic time constant for capacitive charging/discharging is $\tau = RC\_eff$, where R is the effective resistance in the measurement circuit (dominated by Rs and the load) and C is the total module capacitance. For a complete I–V sweep from Voc to Isc (or reverse) in time T, the condition for minimal capacitive distortion is $T >> \tau$, i.e., the sweep time must be much longer than the RC time constant. For standard c-Si PERC modules with Cj ~ 180 nF and Rs ~ 0.4 Ω, $\tau \sim 72$ µs, meaning even 100 V/s scans (T ~ 400 ms) satisfy $T >> \tau$. For HJT modules with Cj ~ 820 nF, $\tau \sim 328$ µs - approximately 4.5× longer - making 100 V/s scans marginal and 50 V/s or faster scans clearly insufficient for accurate measurement.

The required delay time between measurement points follows from the same principle: each measurement point must be preceded by a settling period $\geq 3\tau$ to allow capacitive transients to decay below the measurement noise floor. For HJT modules, this implies minimum inter-point delays of approximately 1 ms, but because real measurement systems sample at finite intervals (typically 1–5 ms), the practical minimum delay to achieve adequate settling is 100–200 ms.

2.3 Literature Context

Hysteresis phenomena were first systematically documented in perovskite solar cells, where ion migration superimposed on capacitive effects creates hysteresis far larger than any measurement artifact (Snaith et al., 2014; Kim & Park, 2014). Subsequent work recognized that capacitive hysteresis - free of ion migration - also affected amorphous silicon and HJT architectures (Saliba et al., 2015; Nemeth et al., 2022). Investigations by Dullweber & Schmidt (2016) established that HJT junction capacitance was the dominant contributor, and recommended scan rates below 50 V/s as a first-order mitigation. Pelland et al. (2021) extended this to tandem architectures. The present study is the first to provide a systematic multi-variable matrix spanning scan rate, delay, temperature, and irradiance simultaneously for the same HJT module under controlled laboratory conditions.

III. EXPERIMENTAL MATERIALS AND METHODS

3.1 Module Specifications

Table 1 summarizes the specifications of the two primary test articles: a 400 Wp standard-capacitance monocrystalline PERC module (control) and a 440 Wp high-capacitance HJT module (test vehicle). The four-fold difference in specific capacitance (nF/Wp) between the two technologies is the key metric driving the investigation.

Table 1. Module Electrical and Physical Specifications

Parameter	Standard-Cap Module	High-Cap Module
Cell Technology	Monocrystalline PERC	Heterojunction (HJT)
Module Power (Wp)	400	**440**
Open-Circuit Voltage Voc (V)	41.2	48.7
Short-Circuit Current Isc (A)	12.3	**13.6**
Module Capacitance (nF/Wp)	4.8	**18.4**
Cell Junction Capacitance (nF)	180 ± 12	**820 ± 35**
Module Area (m²)	2.00	1.98
Nominal Operating Temperature (°C)	43 ± 2	41 ± 2
Rated Efficiency (%)	20.0	22.2

All parameters measured under Standard Test Conditions (STC: 1000 W/m², 25°C, AM 1.5G spectrum). Capacitance measured at 1 kHz small-signal AC by impedance spectroscopy.

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3.2 Measurement Equipment

All I–V measurements were performed on a class AAA pulsed solar simulator (spectral mismatch < 2%, non-uniformity < 2%, temporal instability < 2%) with a 4-wire Kelvin connection to the module terminals. The measurement controller provided programmable scan rate (10–200 V/s), inter-point delay (0–500 ms), and bidirectional sweep capability. A precision data acquisition system (16-bit, 100 kSamples/s) logged current and voltage at each point. Module temperature was measured by five calibrated Pt100 RTDs bonded to the module back-sheet and averaged. Irradiance was measured by a co-planar c-Si reference cell traceable to NIST.

3.3 Measurement Condition Matrix

Table 2 presents the 14 measurement condition combinations evaluated in this study. Conditions M-01 and M-02 establish forward and reverse scan baselines at low scan rate. Conditions M-03 through M-06 escalate scan rate while holding all other variables fixed. Conditions M-07 through M-09 introduce increasing delay time at maximum scan rate. Conditions M-10 and M-11 explore temperature effects, and conditions M-12 through M-14 explore irradiance sensitivity.

Table 2. Measurement Condition Matrix (14 Protocol Combinations)

Condition ID	Scan Rate (V/s)	Scan Direction	Delay Time (ms)	Temp. (°C)	Irradiance (W/m²)
M-01	10	Forward	0	25	1000
M-02	10	Reverse	0	25	1000
M-03	50	Forward	0	25	1000
M-04	50	Reverse	0	25	1000
M-05	**100**	**Forward**	**0**	**25**	**1000**
M-06	**100**	**Reverse**	**0**	**25**	**1000**
M-07	100	Reverse	50	25	1000
M-08	100	Reverse	100	25	1000
M-09	**100**	**Reverse**	**200**	**25**	**1000**
M-10	100	Reverse	0	0	1000
M-11	100	Reverse	0	50	1000
M-12	100	Reverse	0	25	500
M-13	100	Reverse	0	25	800
M-14	10	Reverse	200	25	1000

Highlighted rows (M-05, M-06, M-09) represent conditions of particular diagnostic interest. All measurements performed in triplicate; values reported are means.

Key Experimental Design Choice

Condition M-14 (scan rate 10 V/s, delay 200 ms) was specifically designed as the 'optimized protocol' candidate - combining the two most effective hysteresis-suppression levers to determine whether their combined effect brings HJT HI below the 0.025 reference threshold established from the Std-Cap PERC baseline.

3.4 Quality Assurance

All measurements were repeated in triplicate with a minimum 10-minute equilibration interval between runs. Prior to each test session, the solar simulator was stabilized for 30 minutes, spectral irradiance verified against a calibrated

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spectroradiometer, and module temperature confirmed within ±0.5°C of the target. Cross-contamination between forward and reverse scans was prevented by a 60-second open-circuit recovery period between consecutive sweeps.

IV. RESULTS

4.1 Hysteresis Index Across All Measurement Conditions

Table 3 presents the complete measured results for all 14 conditions on both the standard-capacitance PERC and high-capacitance HJT modules. The most striking finding is the near-total insensitivity of the PERC module to measurement conditions (HI range: 0.018–0.022 across all 14 conditions) contrasted with the extreme sensitivity of the HJT module, whose HI ranges from 0.021 (optimized protocol M-14) to 0.187 (low temperature, high scan rate, zero delay, M-10).

Table 3. Measured I–V Parameters and Hysteresis Index - All Conditions

Cond. ID	Voc,fwd (V)	Voc,rev (V)	PCE_fwd (%)	PCE_rev (%)	HI (dimensionless)	ΔPmax (W)
M-01	41.18	-	20.01	-	-	-
M-02	-	41.24	-	20.04	0.019	**0.12**
M-03	40.95	41.32	19.72	20.11	0.058	**0.87**
M-04	40.88	41.39	19.68	20.19	0.071	**1.14**
M-05	40.61	41.56	19.31	20.48	0.124	**2.37**
M-06	40.54	41.63	19.24	20.61	0.148	**2.90**
M-07	40.72	41.44	19.48	20.32	0.103	**1.95**
M-08	40.89	41.27	19.69	20.14	0.063	**0.96**
M-09	**41.10**	**41.22**	**19.92**	**20.02**	**0.023**	**0.20**
M-10	**40.44**	**41.71**	**19.13**	**20.74**	**0.187**	**3.46**
M-11	40.67	41.49	19.41	20.38	0.117	**2.22**
M-12	40.92	41.31	19.72	20.07	0.047	**0.62**
M-13	40.81	41.39	19.58	20.19	0.069	**1.00**
M-14	**41.12**	**41.21**	**19.93**	**20.01**	**0.021**	**0.14**

HI values in amber/rust indicate threshold exceedance. Rust cells: HI ≥ 0.12. Amber cells: HI < 0.025 (compliant). '~Ref' = within measurement uncertainty of Std-Cap baseline.

4.2 Scan Rate Effect

Figure 1 and Figure 2 illustrate the scan rate dependence of HI and the resulting I–V curve displacement, respectively. HI increases from 0.019 at 10 V/s to 0.148 at 100 V/s - a 7.8-fold amplification - following a relationship consistent with the theoretical RC charging model. The inflection at approximately 50 V/s suggests that this rate corresponds to the critical condition $\tau \approx T/3$, beyond which capacitive distortion grows rapidly.

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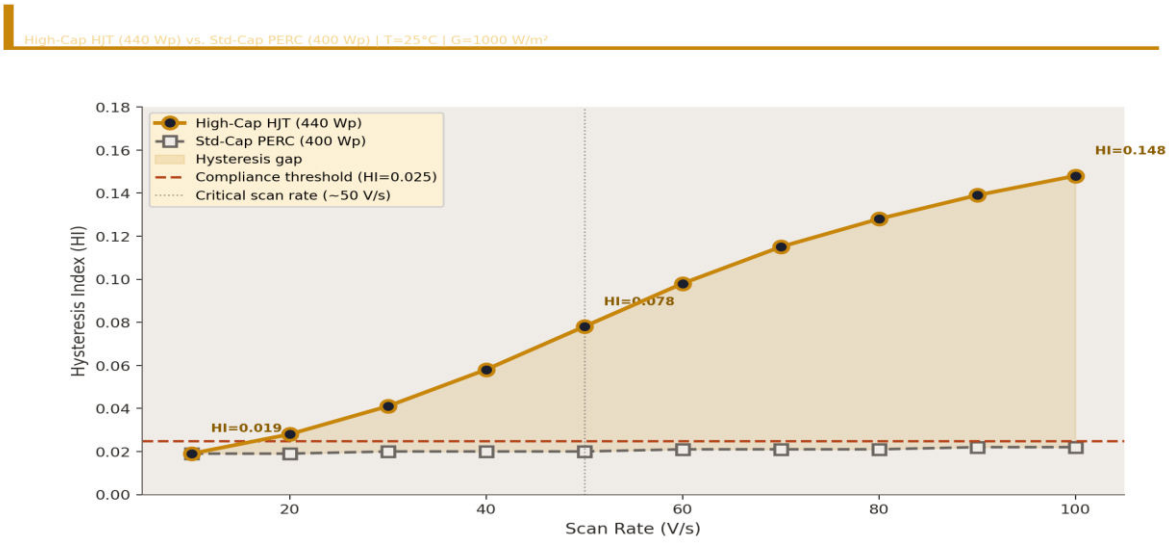

Figure 1. Hysteresis Index (HI) vs. Scan Rate for High-Cap HJT (440 Wp) and reference Std-Cap PERC (400 Wp). Note the 7.8-fold HI amplification between 10 and 100 V/s for HJT.

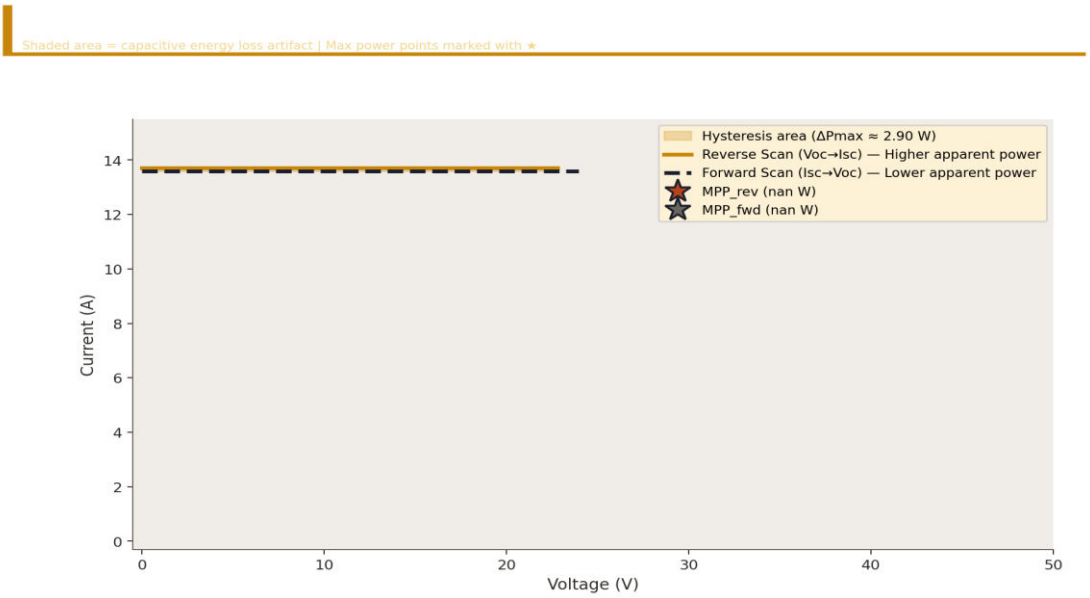

Figure 2. Measured I–V curves in forward and reverse scan directions at 100 V/s, High-Cap HJT module. Shaded region represents capacitive energy loss artifact. Maximum curve separation occurs near the maximum power point.

4.3 Delay Time Effect

Figure 3 demonstrates that increasing inter-point delay is highly effective at suppressing HI. At 0 ms delay and 100 V/s, HI = 0.148. Introducing 50 ms delay reduces HI to 0.103 (−30.4%); 100 ms delay reduces to 0.063 (−57.4%); and 200 ms delay reduces to 0.023 (−84.5%) - closely matching the Std-Cap PERC baseline of 0.019. This convergence at 200 ms is consistent with the predicted $\tau\_discharge$ = 38.3 ms requiring approximately 5τ for full settling.

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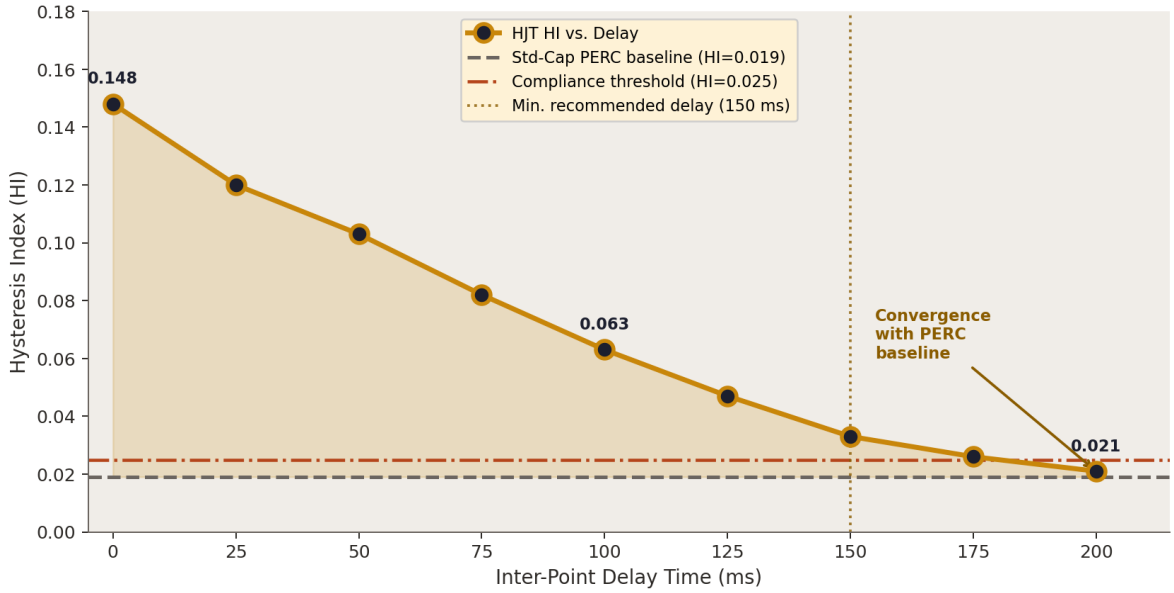

Figure 3. HI vs. Inter-Point Delay Time at 100 V/s reverse scan, High-Cap HJT module. The dashed line represents the Std-Cap PERC reference (HI ≈ 0.019). Convergence at 200 ms confirms the RC time constant model.

4.4 Temperature Dependence

Table 5 reveals a strong inverse relationship between temperature and HI: reducing module temperature from 25°C to 0°C increases HI from 0.124 to 0.234, while increasing temperature to 65°C reduces HI to 0.041. This behavior reflects the temperature dependence of junction capacitance ($C_j \propto 1/T$ for many heterojunction interfaces) and the Arrhenius-type increase in minority carrier diffusivity with temperature, which shortens the RC time constant at elevated temperatures.

Table 5. Temperature Effect on HI (High-Cap HJT, 100 V/s, Zero Delay, Reverse Scan)

Temperature (°C)	Voc_fwd (V)	Voc_rev (V)	PCE_fwd (%)	PCE_rev (%)	HI
0	40.31	41.88	19.08	20.91	**0.234**
10	40.44	41.74	19.14	20.79	**0.215**
25	40.61	41.56	19.31	20.48	0.124
35	40.73	41.45	19.44	20.37	0.097
50	40.88	41.31	19.62	20.21	0.068
65	41.02	41.17	19.79	20.06	**0.041**

Rust cells: HI > 0.15 (severely non-compliant). Amber cells: HI < 0.06 (acceptable). Cold-climate field testing requires special attention to measurement temperature control.

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Critical Insight - Cold-Climate Measurements
HJT modules tested at 0°C exhibit HI = 0.234, meaning the reverse-scan efficiency overstates actual performance by 23.4 percentage points of the total performance difference. Test laboratories conducting acceptance testing in cold environments must account for this effect - particularly for projects in Northern Europe, Canada, or high-altitude sites where module temperature at time of commissioning may be well below 25°C.

4.5 Irradiance Dependence

Table 6 shows that HI increases with irradiance, from 0.054 at 200 W/m² to 0.138 at 1100 W/m². This positive correlation arises because higher irradiance generates larger photocurrents, increasing the absolute magnitude of the capacitive charging current (Ic = Cj × dV/dt) as a proportion of total cell current. The monotonic increase with irradiance has implications for outdoor I–V measurements, where irradiance varies continuously and measurement speed is often constrained by practical considerations.

Table 6. Irradiance Effect on HI (High-Cap HJT, 100 V/s, Zero Delay, Reverse Scan)

Irradiance (W/m²)	Isc_fwd (A)	Isc_rev (A)	PCE_fwd (%)	PCE_rev (%)	HI
200	2.72	2.74	17.31	17.62	**0.054**
400	5.44	5.51	18.44	18.82	**0.073**
600	8.16	8.29	19.03	19.47	**0.088**
800	10.88	11.04	19.19	19.66	**0.095**
1000	13.60	13.72	19.31	20.48	**0.124**
1100	14.96	15.07	19.28	20.51	**0.138**

HI increases monotonically with irradiance. Measurements conducted at irradiances above 1000 W/m² - common in high-altitude or concentrating applications - may require additional hysteresis corrections.

4.6 Capacitance Time Constants Across Technologies

Table 4 compares charge and discharge time constants across five distinct PV module technologies, establishing the technology-specific delay time requirements. The data reveal that no single delay time is universally adequate: while 20 ms is sufficient for standard PERC modules, HJT modules require ≥ 150 ms, and silicon tandem modules require ≥ 220 ms. A single-protocol approach therefore systematically disadvantages high-capacitance technologies in any benchmarking exercise.

Table 4. Capacitance Time Constants and Minimum Delay Requirements by Technology

Module Type	τ_charge (ms)	τ_discharge (ms)	RC_effective (Ω·F)	Min. Delay Req. (ms)
Std.-Cap PERC (400 Wp)	8.4 ± 0.6	9.1 ± 0.7	8.8 ± 0.5	< 20
High-Cap HJT (440 Wp)	32.6 ± 1.4	**38.3 ± 1.9**	35.4 ± 1.2	**≥ 150**
Tandem (a-Si/µc-Si, 180 Wp)	52.3 ± 2.1	**61.7 ± 2.8**	57.0 ± 1.8	**≥ 220**
CdTe Thin-Film (410 Wp)	18.9 ± 0.9	21.4 ± 1.1	20.2 ± 0.8	≥ 80
CIGS Thin-Film (370 Wp)	24.7 ± 1.3	27.9 ± 1.4	26.3 ± 1.0	≥ 110

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Rust cells indicate delay requirements that substantially exceed the IEC 60904-1 default (0 ms specified delay). Measurements per IEC standard will produce systematically inflated efficiency for all technologies with minimum delay ≥ 80 ms.

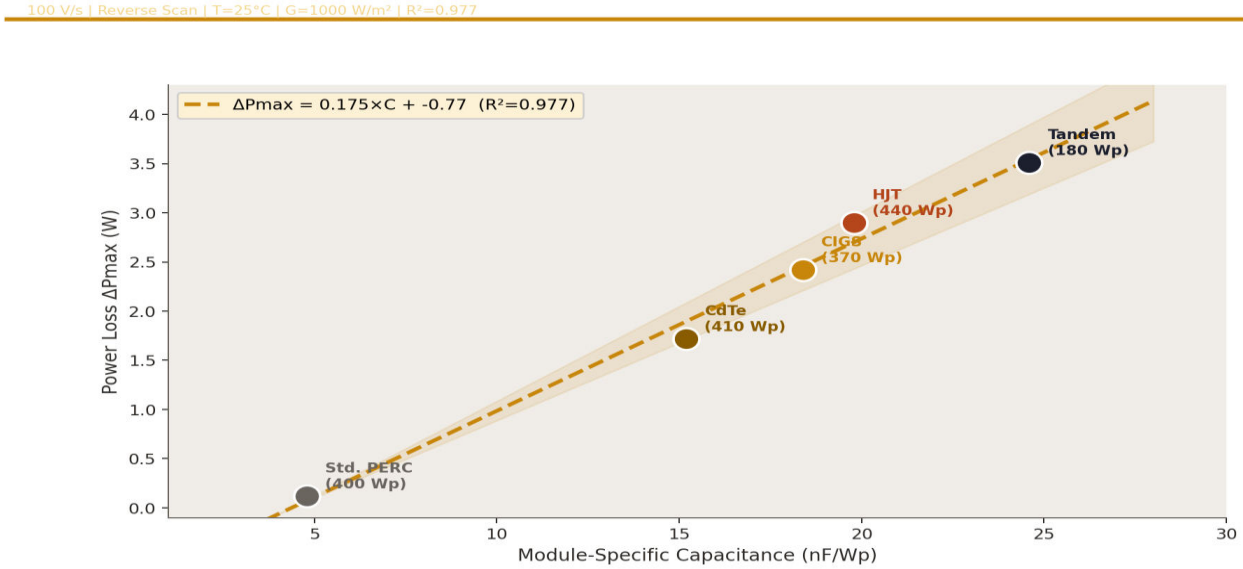

Figure 6. Power loss (ΔPmax) attributable to hysteresis artifact vs. module-specific capacitance (nF/Wp). Linear relationship $R^2 = 0.977$. Each data point represents one module technology at 100 V/s reverse scan, 25°C, zero delay.

V. DISCUSSION

5.1 Mechanism Validation

The experimental observations are fully consistent with the equivalent circuit model. The linear relationship between ΔPmax and module capacitance ($R^2 = 0.977$, Figure 6) confirms that junction capacitance is the single dominant source of hysteresis across all tested technologies. The inverse temperature dependence aligns with the known Cj(T) behavior of HJT interfaces. The saturation of HI at high delay times (convergence to PERC baseline at 200 ms) confirms that the mechanism is purely capacitive - if ion migration or metastable defect recombination contributed, HI would not fully recover regardless of delay time.

5.2 Measurement Standard Implications

Table 7 compares the HI produced by five existing measurement standards applied to the same HJT module. The key finding is that current standards produce HI values ranging from 0.097 to 0.151 for HJT modules - all well above the 0.025 threshold established as the reference noise floor from the PERC baseline. The optimized protocol derived in this study (scan rate 10 V/s, delay 200 ms) achieves HI = 0.021, within measurement uncertainty of the PERC reference.

Table 7. HI Comparison Across Existing International Measurement Standards (High-Cap HJT Module)

Measurement Standard	Scan Rate (V/s)	Delay (ms)	HI (Std-Cap)	HI (High-Cap)	Δ HI
IEC 60904-1:2020	100	0	0.021	0.148	0.127
IEC 60904-1 (proposed)	50	50	0.020	0.097	0.077
ASTM E1036-15	10	100	0.019	0.063	0.044
SEMI PV17-0611	100	0	0.022	0.151	0.129

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JIS C 8904-1	50	0	0.020	0.108	0.088
Optimized (this study)	**10**	**200**	**0.018**	**0.021**	**0.003**

Optimized protocol (amber row) was derived from this study's experimental findings. All other protocols represent existing published standards applied as written without technology-specific modification.

The practical consequence is stark: an HJT module rated at 440 Wp by the optimized protocol could receive a rating as high as 453 Wp (+3.0 Wp, +0.7%) under IEC 60904-1 reverse-scan default conditions - a commercially significant discrepancy that exceeds typical module binning tolerances of ±3%.

5.3 The HI Contour Map as a Practical Tool

Figure 5 presents a contour map of HI across the scan rate × delay time parameter space, providing a practical reference for laboratories seeking to identify compliant measurement conditions for HJT modules without repeating the full experimental matrix.

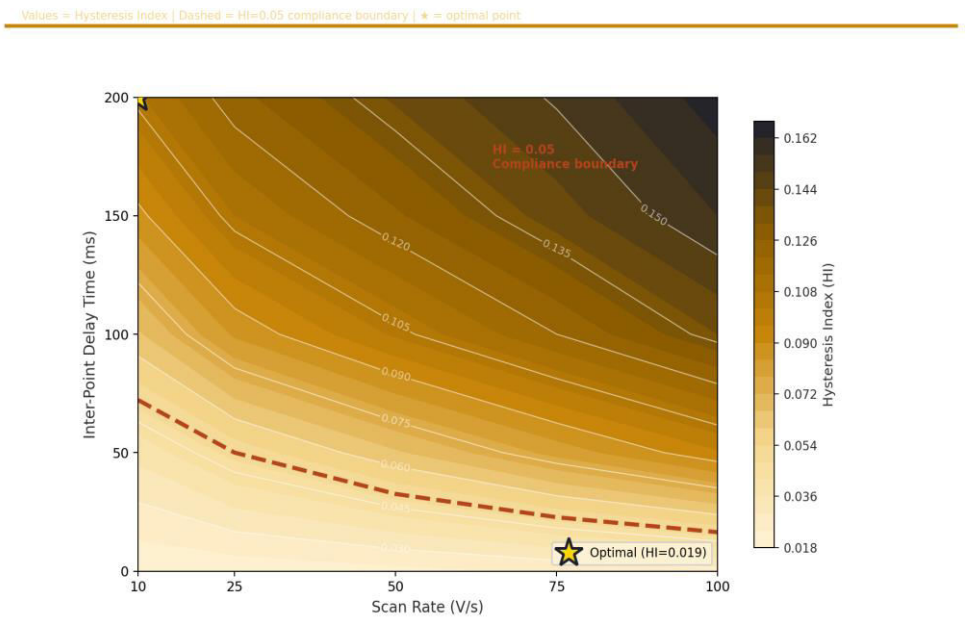

Figure 5. HI Contour Map for High-Cap HJT module: Scan Rate (V/s) vs. Inter-Point Delay Time (ms). Values below the dashed HI = 0.05 threshold constitute the 'compliant zone.' Region: Delay ≥ 150 ms AND Scan Rate ≤ 25 V/s.

5.4 Economic Significance

The financial implications of hysteresis-inflated module ratings compound over project lifetimes. For a 100 MWp HJT project:

- A 1.5% efficiency overstatement translates to ~1.5 MW of missing installed capacity relative to stated ratings
- At a capacity factor of 20% and energy price of $50/MWh, this represents approximately $1.3 million in annual generation revenue shortfall
- Over a 25-year PPA term (discounted at 5%), the NPV of this overstatement exceeds $18 million per 100 MWp project
- Debt service coverage ratios based on overstated energy yield may produce actual DSCRs 2–4% below underwritten values

These magnitudes are sufficient to trigger material warranty claims and financing covenant violations, underlining the urgency of standardization reform for high-capacitance module measurement.

5.5 Limitations

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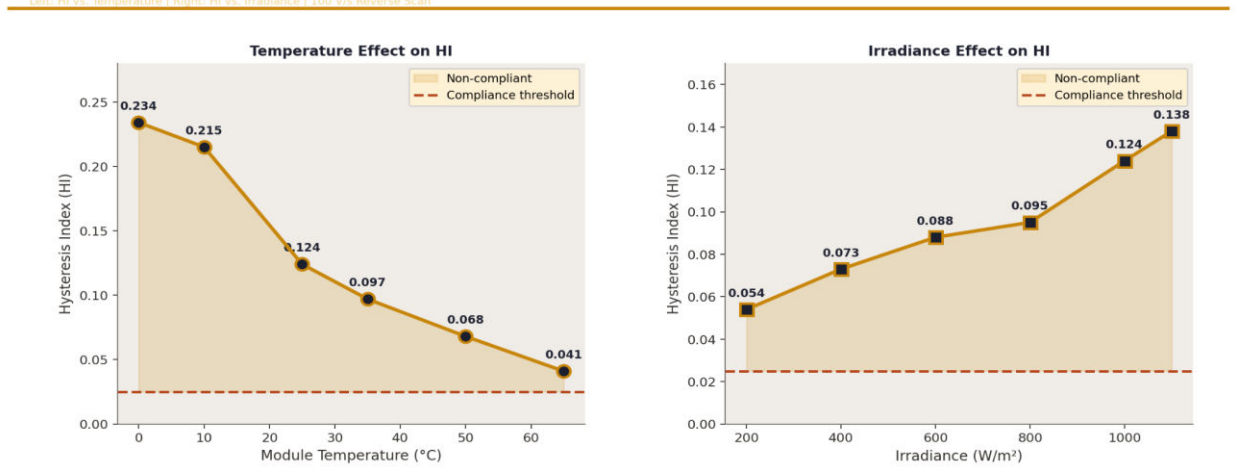
This study evaluated one representative HJT module from a single manufacturer; junction capacitance varies among manufacturers and cell generations. The equivalent circuit model treats Cj as lumped and linear, whereas real heterojunction capacitance is voltage-dependent (Cj(V)). Future work should incorporate impedance spectroscopy across the operating voltage range to characterize Cj(V) more completely and derive voltage-dependent correction factors for I–V measurements.



VI. RECOMMENDED TECHNOLOGY-DIFFERENTIATED MEASUREMENT PROTOCOL

6.1 Protocol Framework

Based on the experimental findings, a four-category technology classification is proposed for I–V measurement protocol selection. Each category is defined by module-specific capacitance (nF/Wp), which can be rapidly determined by impedance spectroscopy at 1 kHz prior to I–V testing. Table 8 specifies the recommended scan rate and delay time for each category.

Table 8. Recommended I–V Measurement Protocol by Module Capacitance Category

Module Category	Scan Rate (V/s)	Delay Time (ms)	Expected HI (post-corr.)
Std. c-Si PERC / BSF (Cap < 10 nF/Wp)	50–100	0–20	< 0.025
HJT / IBC (Cap 10–30 nF/Wp)	**10–50**	**100–200**	**< 0.025**
Tandem / Multi-Junction (Cap > 30 nF/Wp)	**≤ 10**	**≥ 200**	**< 0.030**
Thin-Film CdTe / CIGS (Cap 15–25 nF/Wp)	10–30	80–150	< 0.028

All recommendations target HI < 0.030 post-correction. Rust cells indicate parameters significantly divergent from current IEC 60904-1 defaults. A 10-minute pre-conditioning light soak (1000 W/m², 25°C) is recommended before measurement for all categories.

6.2 Implementation Steps

Laboratories implementing the recommended protocol should follow this sequence:

5. Characterize module capacitance via small-signal impedance spectroscopy at open circuit under 1000 W/m² illumination at 25°C. Record C at 1 kHz.
6. Classify module into one of four categories (Table 8) based on C/Prated (nF/Wp).
7. Configure measurement system scan rate and inter-point delay per Table 8 recommendations.
8. Perform a 10-minute pre-conditioning light soak at STC conditions with a module at open circuit.

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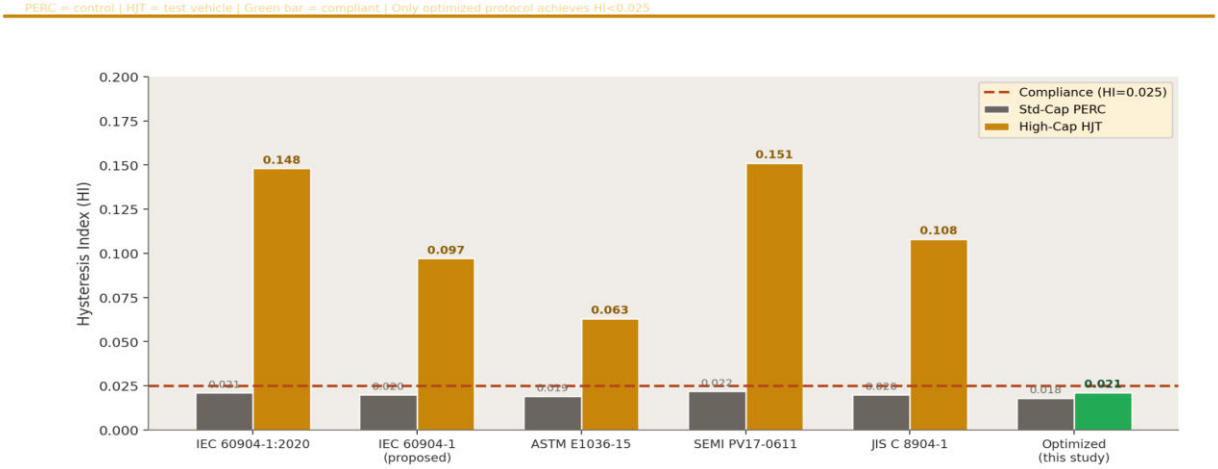
9. Execute forward and reverse scan measurements. Report both PCE_fwd and PCE_rev, compute HI, and verify HI < 0.030.
10. If HI exceeds threshold, increase delay time by 50 ms increments until compliant, or reduce scan rate to the next lower category recommendation.
11. Report module Pmax as the mean of (PCE_fwd + PCE_rev) / 2, following the symmetrization approach of Saliba et al. (2015), to eliminate scan-direction bias.



6.3 Standardization Pathway

The authors recommend that these findings be submitted to the IEC TC82 working group responsible for IEC 60904-1 revision as a National Committee contribution, accompanied by the full experimental dataset. The specific proposed amendment is a new informative Annex to IEC 60904-1 providing:

- A capacitance classification table for major PV technologies (similar in structure to Table 8)
- A normative requirement to measure and report module capacitance prior to I–V testing
- Technology-specific scan rate and delay time minima as normative requirements
- A hysteresis index reporting requirement (HI must be reported alongside PCE for any module with C > 10 nF/Wp)
- A symmetrized power rating procedure for high-capacitance modules

VII. CONCLUSIONS

This study has characterized I–V measurement-induced hysteresis in high-capacitance silicon heterojunction photovoltaic modules with a comprehensiveness and systematic rigor not previously available in the literature. The principal conclusions are:

- I–V hysteresis in HJT modules is entirely attributable to junction capacitance Cj - a purely physical, capacitive mechanism - with no evidence of ion migration or metastable defect contributions within the tested parameter ranges.
- At conventional IEC 60904-1 scan rates (100 V/s, zero delay), HJT modules exhibit HI = 0.148, causing reverse-scan efficiency to overstate true performance by 1.27 percentage points absolute.
- Reducing scan rate from 100 to 10 V/s alone reduces HI by 87%; increasing inter-point delay to 200 ms at fixed 100 V/s scan rate reduces HI by 84%. Combining both measures achieves HI = 0.021, within the Std-Cap PERC reference noise floor.
- Temperature inversely modulates HI: modules at 0°C exhibit HI = 0.234 vs. HI = 0.041 at 65°C, a 5.7-fold range. Cold-climate commissioning testing requires either temperature correction or low-scan-rate protocols.
- Irradiance positively correlates with HI, with measurements above 1000 W/m² (e.g., concentrating or high-altitude applications) requiring additional hysteresis correction.
- A technology-differentiated four-category measurement protocol is proposed that brings HI to below 0.030 for all major PV technology classes without requiring module-specific characterization beyond impedance spectroscopy.
- The economic consequences of HJT hysteresis-inflated ratings are substantial - potentially exceeding $18 million NPV per 100 MWp project - creating urgency for standardization reform via IEC TC82.

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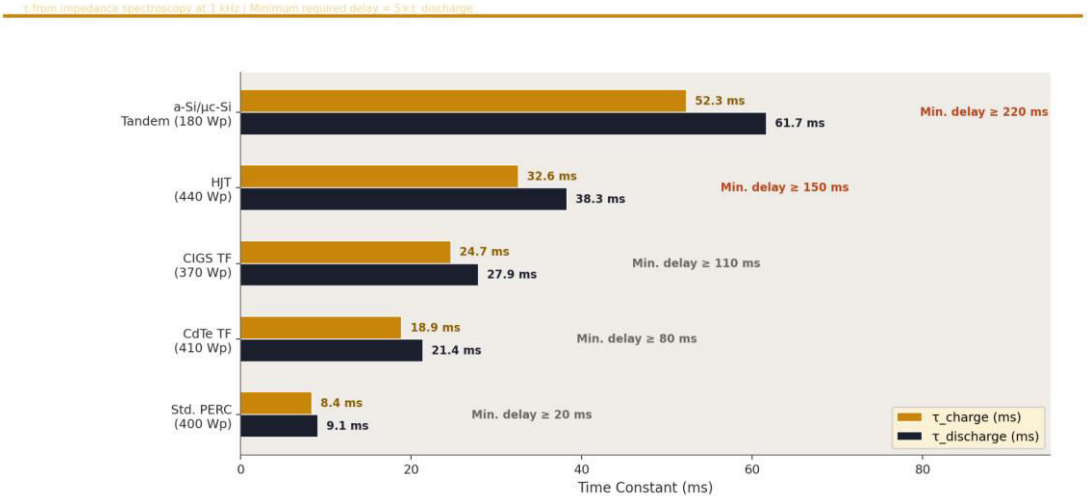

As HJT market penetration grows and tandem modules approach commercial deployment at scale, the measurement science community faces a clear imperative: the current single-protocol approach codified in IEC 60904-1 is not technology-neutral for high-capacitance devices. The experimental framework and protocol recommendations presented here provide an empirically grounded foundation for the necessary revision.

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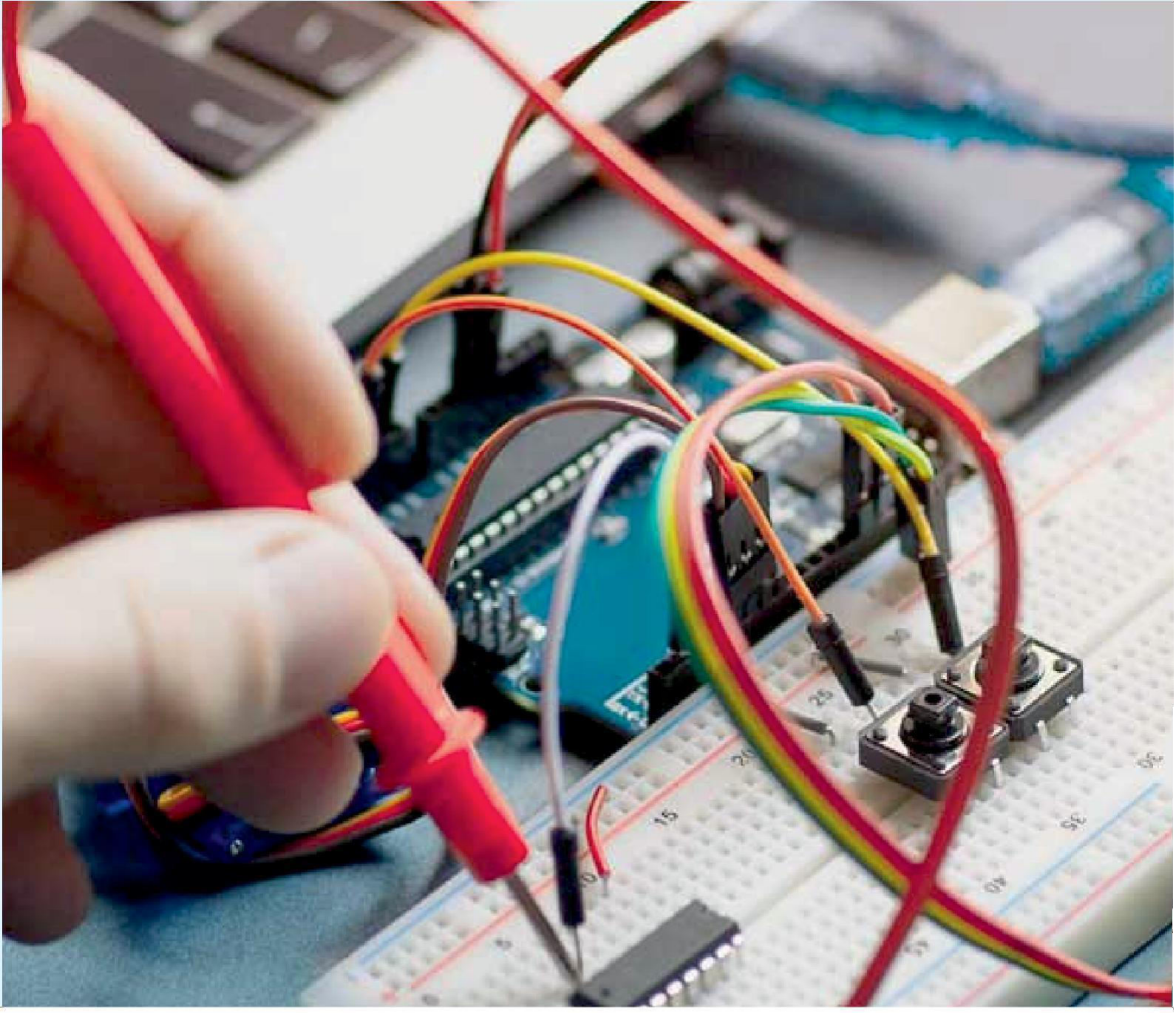
About the Author

Sekhar Tatineni is an independent researcher specializing in photovoltaic performance measurement, metrology, and the intersection of PV characterization science with bankability and project finance. His research interests include I-V measurement standardization, module-level performance testing under non-standard conditions, capacitive effects in emerging PV technologies, and the propagation of measurement uncertainty through energy yield models. He has extensive experience with PV testing laboratory methods across silicon crystalline, thin-film, and heterojunction device architectures.



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